UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/844,673 | 04/30/2001 | Radhika Thekkath | MTEC006/00US | 8988 |

22903 7590 07/22/2004

COOLEY GODWARD LLP
ATTN: PATENT GROUP
11951 FREEDOM DRIVE, SUITE 1700
ONE FREEDOM SQUARE- RESTON TOWN CENTER
RESTON, VA 20190-5061

| EXAMINER | |
|---|---|
| RUTTEN, JAMES D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2122 | |

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/844,673 | THEKKATH, RADHIKA | |
| | Examiner | Art Unit | |
| | J. Derek Rutten | 2122 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3, 5-13, and 15-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-3,5-13 and 15-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Acknowledgement is made of Applicants' amendment dated April 19, 2004 responding to the November 14, 2003 Office Action provided in the rejection of claims 1-24, wherein claims 1-3, 5-7, 10-13, 15-22, and 24 have been amended, and claims 4 and 14 were canceled. Claims 1-3, 5-13, and 15-24 remain pending in the application and have been fully considered by the examiner.

2. Applicant's arguments, see page 12, filed April 19, 2004, with respect to the rejections of claims 1, 11, 21, 22, and 24 under 35 U.S.C. 102(b) and 103(a) have been fully considered and are persuasive in light of the current amendments. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of U.S. Patent 5,621,886 to Alpert et al. (hereinafter referred to as "Alpert").

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

### *Claim Objections*

4. Claim 10 is objected to because of the following informalities: A typo results in the omission of two additional right parentheses in the last line. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 6 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 6 contains the trademark/trade names MIPS32 and MIPS64. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe 32 and 64 bit embedded processor core architecture specifications and, accordingly, the identification/description is indefinite.

8. Claim 16 contains the trademark/trade names MIPS32 and MIPS64, and suffers the deficiencies noted in the above rejection of claim 6.

***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-3, 5, 7-9, 11-13, 15, 17-22, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Alpert.

As per claim 1, Alpert discloses:

*A tracing method* (column 16 line 39 – column 17 line 25), *comprising:*

*detecting an operating state of a processor, said processor having a plurality of operating states that include a plurality of processor modes* (column 4 lines 16-18 describes operation of a plurality of processor modes. Operating states are inherent since the state of a running processor directly relates to its mode of operation.)*; and*

*effecting a predefined tracing control based on a current operating state of said processor and upon a control input for said current operating state, each particular operating state having a corresponding control input that determines whether tracing is enabled in said particular operating state* (column 4 lines 23-36: "`This first indication indicates` **`which mode the processor is currently`**

**operating in**. The circuit has stored therein a second indication and a third indication. The second indication indicates **whether a debug event is to be recognized** while the processor is operating in the first mode. The third indication indicates whether the debug event is to be recognized while the processor is operating in the second mode. The debug circuitry is coupled to the first storage area to receive the first indication. The debug circuitry is also coupled to the circuit to **receive either the second indication or the third indication based on the state of the first indication**. The debug circuitry allows for the **recognition of the debug event based on the state of the indication** it receives from the circuit."), *whereby tracing control is automatically adjusted when said processor transitions from one operating state to another operating state* (column 5 lines 1-6: "This document describes an invention allowing for the separate enablement of debug events during the execution of operating system routines and non-operating system routines. This allows programmers the flexibility of **selectively enabling debug events** during the execution of either handlers, or applications, or both").

As per claim 2, the above rejection of claim 1 is incorporated. Alpert further discloses: *wherein an indication of said control input for said current operating state is obtained via an input control signal* (column 8 lines 63-67).

As per claim 3, the above rejection of claim 1 is incorporated. Alpert further discloses: *wherein an indication of said control input for said current operating state is obtained via a software-settable trace control register* (column 8 lines 49-51).

As per claim 5, the above rejection of claim 1 is incorporated. Alpert further discloses: *wherein said processor modes comprise at least one of a kernel mode, a supervisor mode, a user mode, and a debug mode* (column 6 lines 1-3).

As per claim 7, the above rejection of claim 1 is incorporated. Alpert further discloses: *wherein said at least one operating state includes an identity of a process being run on said processor and said predefined trace control is based on a current processor mode and said identity of a process* (column 5 lines 55-57; column 6 lines 1-3).

As per claim 8, the above rejection of claim 1 is incorporated. Alpert further discloses: *wherein said effecting comprises initiating tracing* (column 12 lines 9-12).

As per claim 9, the above rejection of claim 1 is incorporated. Alpert further discloses: *wherein said effecting comprises inhibiting tracing* (column 8 line 49 – column 9 line 4 discusses enablement. A lack of enablement would result in inhibitiuon.).

As per claim 11, Alpert discloses a processor core and trace generation logic (Figure 1; also column 5 lines 44-50). All further limitations have been addressed in the above rejection of claim 1.

As per claims 12, 13, and 15, and 17-20, the above rejection of claim 11 is incorporated. All further limitations have been addressed in the above rejections of claims 2, 3, 5, and 7-10, respectively.

As per claim 21, Alpert discloses computer-readable program code (Figure 1, element 122). All further limitations have been addressed in the above rejection of claim 1.

As per claim 22, Alpert discloses transmitting code to a computer, as this is inherent in execution debug software, since a computer needs code in order to execute (Figure 1, element 122). All further limitations have been addressed in the above rejection of claim 1.

As per claim 24, Alpert inherently discloses a data signal embodied in a transmission medium (Figure 1, element 140). All further limitations have been addressed in the above rejection of claim 1.

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert as applied to claims 5 and 15 above, and further in view of "Embedded Processor Watch" by Tom Halfhill (hereinafter referred to as "Halfhill").

As per claim 6, the above rejection of claim 5 is incorporated. Alpert does not expressly disclose implementation based on a 32 or 64 bit embedded processor architecture specification. However, in an analogous environment, Halfhill teaches the availability of embedded processor cores based on 32 and 64 bit architecture specifications (page 1 paragraph 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made implement Alpert's processor modes using Halfhill's teaching of embedded processor specifications. One of ordinary skill would have been motivated to implement an embedded processor for high performance, flexibility, low power consumption, and low cost.

As per claim 16, the above rejection of claim 15 is incorporated. All further limitations have been addressed in the above rejection of claim 6.

13. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert as applied to claim 1 above, and further in view of "MIPS R10000 Microprocessor User's Manual" by MIPS Technologies, Inc. (hereinafter referred to as "R10000").

As per claim 10, the above rejection of claim 1 is incorporated. Alpert further discloses: *wherein said operating states include an identity of a process running on said processor and tracing is triggered based on ASID, U, and K, controls, wherein trace data is processed for a current ASID value, ASID is an application space identity, U, if asserted, enables tracing in user mode, K, if asserted enables tracing in kernel mode, said controls enabling tracing when:*

*( (ASID equals a current process application space identity value) AND*

*( (U is asserted AND said processor is in user mode) OR*

*(K is asserted AND said processor is in kernel mode)))*

Alpert does not expressly disclose *G, S, DM, and X controls, wherein said G if asserted implies that all processes are to be traced, whereas if G is not asserted, trace data is processed for a current ASID value, S, if asserted, enables tracing in supervisor mode, DM, if asserted, enable tracing in a debug mode, and X, if asserted, enables tracing for exception and error level conditions, said controls enabling tracing when:*

*((G is asserted) AND*

*( (S is asserted AND said processor is in supervisor mode) OR*

*(DM is asserted AND said processor is in debug mode) OR*

*(X is asserted AND (an exception level bit is asserted OR an error level bit is asserted))))*.

However, in an analogous environment, R10000 teaches a processor that runs using three modes including a supervisor mode in addition to a user and kernel mode (page 316 – Section 16.1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teaching of R10000 to enable the use of multiple modes of operation within Alpert's processor. One of ordinary skill would have been motivated to enable fine-grained control of an application or system process using multiple operating modes and debug conditions.

As per claim 20, the above rejection of claim 11 is incorporated. All further limitations have been addressed in the above rejection of claim 10.

14. Claims 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert.

As per claim 23, the above rejection of claim 22 is incorporated. Alpert does not expressly disclose transmitting via the internet. However, official notice is taken, since

the Internet is a well-known medium for exchanging data between computer systems in different physical locations.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Derek Rutten whose telephone number is (703) 605-5233. The examiner can normally be reached on M-F 6:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jdr

TUAN DAM
SUPERVISORY PATENT EXAMINER